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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CORRIELUS, JEAN B	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,669	EICHRODT ET AL.	
	Examiner	Art Unit	
	Jean B. Corrielus	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-38 and 40-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-38,40-46 and 48-53* is/are rejected.

7)☒ Claim(s) *47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/16/08 has been entered.

Drawings

2. Applicant's argument with respect to the drawing objection is persuasive the outstanding drawing objection has been withdrawn.

Specification

3. The substitute specification filed 5/16/08 has been entered

Claim Objections

4. Claims 40 and 46 are objected to because of the following informalities: claim 40 depends on canceled claim 39, it appears that the dependency should have been "38" rather than "39". The claim will not be rejected/objected at this time as being incomplete. The claim will be treated as being dependent on claim 38. Applicant is required to amend the claim as indicated above or in an appropriate manner to correct the dependency error. Claim 46 depend on claim 41, it appears that that applicant intended to make claim 46 dependent on claim 44. For examination purpose, the claim will be considered as being dependent on claim 44 rather than claim 41. Applicant is

required to amend the claim as indicated above or in an appropriate manner to correct the dependency error. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 37 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

"the step of monitoring a data signal", recited in claim 37 lack of proper antecedent basis.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 35, 37, 38 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minagawa US patent No. 6,023,774 in view of Chang US patent No. 4,434,403.

As per claim 35, Minagawa discloses a method comprising determining whether a data signal exhibits a change in value see for instance fig. 6 circuit 21 and fig. 1 and generating a first signal (i.e. turn off see col. 10, line 48) in response to determining that the data signal does not exhibit a change in value see col. 10, lines 47-50, col. 11, lines 10-15, col. 13, lines 6-12. Note that because of turnoff condition, no current is flowing in Minagawa accordingly, no DC condition exists. Hence the turn off signal results inherently in preventing any DC flow condition. However, Minagawa does not teach the additional limitation of monitoring a clock signal and generating a signal in response to a clock signal condition to prevent the DC flow condition. Chang teaches monitoring a clock signal and generating a signal in response to a clock signal condition see abstract, lines 1-3. Note that by providing a reset signal any DC condition that may exist in Chang would have been inherently reset or prevented since the circuit would have been re-initialized in response to the reset signal. It would have been obvious to one skill in the art to incorporate such a teaching in Minagawa in order to provide Minagawa with the capability to detect clock failure so that proper compensation can be provided because clock errors in signal communication if not compensated for may result in data misdetection or even data lost.

As per claim 37, as evidence by Chang see abstract, it is well known in the art to include a comparator in a monitoring device. Given that fact, it would have been obvious

to one skill in the art to incorporate a comparator device in the monitoring device because comparator circuits are easier to implement and readily available.

As per claim 38 the first signal is a turnoff (power down signal) see col. 10, line 48.

As per claim 41, Chang teaches the second signal is a reset signal see abstract, lines 1-3. One skill in the art would have been motivated to implement the second signal as a "reset signal" as taught by Chang for the reason provided above with respect to claim 35.

9. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minagawa US patent No. 6,023,774 in view of Chang US patent No. 4,434,403 and further in view of Kodra US Patent No. 6,226,663.

10. As applied to claim 35 above, Minagawa and Chang teach every feature of the claimed invention but do not explicitly teach the further limitation of a sigma delta modulator configured to provide the data signal. Kodra teaches a sigma delta modulator 12 configured to provide the data signal to monitor 22. Given that fact, it would have been obvious to one skill in the art to use a sigma delta modulator in Minagawa and Chang to produce the data signal so as to take advantage of the inherent property of the sigma delta modulator which makes the probability of encountering a long string of consecutive ones or zeroes during nominal operation to be very small.

11. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minagawa US patent No. 6,023,774 in view of Chang US patent No. 4,434,403 US Patent No. 4,353,128 and further in view of Hicks US Patent No. 4,800,562.

12. As applied to claim 39 above, Minagawa and Chang teach every feature of the claimed invention but do not explicitly teach the further limitation power down is generated by an asynchronous counter that reaches a maximum value. Hicks teaches further limitation power down is generated by an asynchronous counter that reaches a maximum value see col. 2, lines 42-52. Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Minagawa and Chang in order to prevent the system from processing invalid data signal and at the same time to minimize power consumption.

13. Claims 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minagawa US patent No. 6,023,774 in view of Chang US patent No. 4,434,403 and further in view of Buer US Patent No. 6,188,257.

14. As per claim 42, as applied to claim 35 above, Minagawa and Chang teach every feature of the claimed invention but do not explicitly teach the further limitation generating the reset signal in response to a clock signal having a frequency that fails to exceed a predetermined minimum value. Buer teaches the further limitation of generating the reset signal in response to a clock signal having a frequency that fails to exceed a predetermined minimum value. See col. 1, line 65-col. 2, line 2. It would have been obvious to one skill in the art to incorporate such a teaching in Minagawa and Chang in order to prevent the system from processing invalid data signal and at the same time to minimize power consumption.

15. As per claim 43, Minagawa Chang and Buer fail to teach the use of a monostable circuit to generate the reset signal. Note however that it is well known in the art to use a

monostable circuit to generate a reset signal. Given that, it would have been obvious to one skill in the art to use a monostable circuit in Minagawa, Chang and Buer to generate the reset signal since such a circuit behaves well with other circuit components and is also easy to implement.

16. Claims 44 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minagawa US patent No. 6,023,774 in view of Hatata et al US patent No. 4,481,629 and further in view of Chang US patent No. 4,434,403.

17. As per claim 44, Minagawa discloses a method comprising determining whether a data signal exhibits a change in value see for instance fig. 6 circuit 21 and fig. 1 and generating a first signal (i.e. turn off see col. 10, line 48) in response to determining that the data signal does not exhibit a change in value see col. 10, lines 47-50, col. 11, lines 10-15, col. 13, lines 6-12,. Note that because of turnoff condition, no current is flowing in Minagawa accordingly, no DC condition exists. Hence the turn off signal results inherently in preventing any DC flow condition. However, Minagawa does not teach the additional limitation of the data signal condition exists if the data signal maintains a present data level beyond a predetermined limit and it further fails to teach monitoring a clock signal and generating a signal in response to a clock signal condition to prevent the DC flow condition. Hatata et al teaches (abstract and col. 2, lines 10-18) a data condition exists if the data signal maintains a present data level (i.e. 3 data levels) beyond a predetermined limit (i.e. 3). Given that fact, it would have been obvious to one skill in the art to incorporate such a teaching in Minagawa in order to provide an

efficient technique to determine communication failure for proper signal compensation. In addition, Chang teaches monitoring a clock signal and generating a signal in response to a clock signal condition see abstract, lines 1-3. Note that by providing a reset signal any DC condition that may exist in Chang would have been inherently reset or prevented since the circuit would have been re-initialized in response to the reset signal. It would have been obvious to one skill in the art to incorporate such a teaching in Minagawa and Hatata in order to provide Minagawa and Hatata with the capability to detect clock failure so that proper compensation can be provided because clock errors in signal communication if not compensated for may result in data misdetection or even data lost.

18. As per claim 52, Minagawa, Hatata, and Chang fail to teach the use of a monostable circuit to generate the reset signal. Note however that it is well known in the art to use a monostable circuit to generate a reset signal. Given that, it would have been obvious to one skill in the art to use a monostable circuit in Minagawa, Hatata, and Chang to generate the reset signal since such a circuit behaves well with other circuit components and is also easy to implement.

19. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minagawa US patent No. 6,023,774 in view of Hatata et al US patent No. 4,481,629 and further in view of Chang US patent No. 4,434,403 and further in view of Kodra US Patent No. 6,226,663.

20. As applied to claim 35 above, Minagawa Hatata and Chang teach every feature of the claimed invention but do not explicitly teach the further limitation of a sigma delta modulator configured to provide the data signal. Kodra teaches a sigma delta modulator 12 configured to provide the data signal to monitor 22. Given that fact, it would have been obvious to one skill in the art to use a sigma delta modulator in Minagawa Hatata and Chang to produce the data signal so as to take advantage of the inherent property of the sigma delta modulator which makes the probability of encountering a long string of consecutive ones or zeroes during nominal operation to be very small.

21. Claim 46 rejected under 35 U.S.C. 103(a) as being unpatentable over Minagawa US patent No. 6,023,774 in view of Hatata et al US patent No. 4,481,629 in view of Chang US patent No. 4,434,403 and further in view of Buer US Patent No. 6,188,257.

As per claim 46, as applied to claim 44 above, Minagawa Hatata and Chang teach every feature of the claimed invention but do not explicitly teach the further limitation generating the reset signal in response to a clock signal having a frequency that fails to exceed a predetermined minimum value. Buer teaches the further limitation of generating the reset signal in response to a clock signal having a frequency that fails to exceed a predetermined minimum value. See col. 1, line 65-col. 2, line 2. It would have been obvious to one skill in the art to incorporate such a teaching in Minagawa Hatata and Chang in order to prevent the system from processing invalid data signal and at the same time to minimize power consumption.

22. Claims 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minagawa US patent No. 6,023,774 in view of Hatata et al US patent No. 4,481,629

further in view of Chang US patent No. 4,434,403 and further in view of Buer US Patent No. 6,188,257.

As per claim 49, Minagawa discloses a method comprising determining whether a data signal exhibits a change in value (monitoring a data signal) see for instance fig. 6 circuit 21 and fig. 1 and generating a turn off signal (power down signal) see col. 10, line 48 in response to determining that the data signal does not exhibit a change in value (all 1's signal levels or all 0's signal levels) (present data level) see col. 10, lines 47-50, col. 11, lines 10-15, col. 13, lines 6-12. However, Minagawa does not teach the additional limitation of the data signal condition exists if the data signal maintains a present data level for a predetermined clock cycles and it further fails to teach monitoring for an anomalous clock signal comprising a clock signal with a frequency that fails to exceed a predetermined minimum value and generating a reset signal if an anomalous clock signal exists. Hatata et al teaches (abstract and col. 2, lines 10-18) a data condition exists if the data signal maintains a present data level (i.e. 3 data levels) beyond a predetermined limit (i.e. 3)(note that in the art of digital signal processing, it is common practice to represent each bit by a clock cycle, see for instance US patent no. 5,805,632 fig. 4 that shows a data bit for each clock cycle). Therefore, one skill in the art would have recognized a three bit limit to be equivalent to a 3 clock cycles limit. Accordingly, one skill in the art would have been motivated to generate the power down signal if the data signal maintains a present data value for a predetermined number of clock cycles in order to provide an efficient technique to determine communication failure for proper signal compensation. In addition, Chang teaches monitoring a clock

signal and generating a signal in response to a clock signal condition see abstract, lines 1-3. It would have been obvious to one skill in the art to incorporate such a teaching in Minagawa and Hatata in order to provide Minagawa and Hatata with the capability to detect clock failure so that proper compensation can be provided because clock errors in signal communication if not compensated for may result in data misdetection or even data lost. Buer teaches the further limitation of generating the reset signal in response to a clock signal having a frequency that fails to exceed a predetermined minimum value. See col. 1, line 65-col. 2, line 2. It would have been obvious to one skill in the art to incorporate such a teaching in Minagawa Hatata and Chang in order to prevent the system from processing invalid data signal and at the same time to minimize power consumption.

As per claim 50, the combined references do not teach the additional limitations of monitoring how long the clock signal remains high and low. However in the art of digital signal processing, it is well known practice to use simple mathematic to determine how long a clock signal remains high and low. Given that, it would have been obvious to one skill in the art to monitor how long the clock signal remains high and low so as to provide a cost efficient technique to determine clock abnormalities.

As per claim 51 it would have been obvious to one skill in the art to monitor whether the clock signal remains high and low beyond a predetermined limit of time and the reason to do so would have been the same as provided above with respect to claim 50.

As per claim 52, Minagawa, Hatata, Chang and Buer fail to teach the use of a monostable circuit to generate the reset signal. Note however that it is well known in the art to use a monostable circuit to generate a reset signal. Given that, it would have been obvious to one skill in the art to use a monostable circuit in Minagawa, Hatata, Chang and Buer to generate the reset signal since such a circuit behaves well with other circuit components and is also easy to implement.

23. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minagawa US patent No. 6,023,774 in view of Hatata et al US patent No. 4,481,629 and further in view of Chang US patent No. 4,434,403 further in view of Buer US Patent No. 6,188,257 and further in view of Kodra US Patent No. 6,226,663.

As per claim 53, as applied to claim 49 above, Minagawa Hatata Chang, Buer teach every feature of the claimed invention but do not explicitly teach the further limitation of a sigma delta modulator configured to provide the data signal. Kodra teaches a sigma delta modulator 12 configured to provide the data signal to monitor 22. Given that fact, it would have been obvious to one skill in the art to use a sigma delta modulator in Minagawa Hatata , Chang and Buer to produce the data signal so as to take advantage of the inherent property of the sigma delta modulator which makes the probability of encountering a long string of consecutive ones or zeroes during nominal operation to be very small.

Allowable Subject Matter

24. Claim 47 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

25. Applicant's arguments filed 5/16/08, with respect to Cummiskey reference has been considered and are persuasive. However, after further consideration a new ground of rejection is set forth above in view of Minagawa.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Corrielus whose telephone number is 571-272-3020. The examiner can normally be reached on Monday-Thursday from 9:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jean B Corrielus/
Primary Examiner
Art Unit 2611